DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/22/2009 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 37 and 39-43 are rejected under 35 U.S.C. 102(b) as being anticipated by Kobayashi et al (US 4,829,022).

Kobayashi et al teaches Group III (Ga) atoms are supplied to the substrate so that one atomic layer is formed by one irradiation of the Ga beam (first crystal raw material) and then atoms of Group V (As) (second raw material) are supplied after the supply of Group III atoms has been completed, whereby the III-V molecules are formed (col 9, ln 25 to col 10, ln 51). Kobayashi et al also teaches the step of doping impurities which is required for the fabrication of various PN junction devices is carried out by supplying p-type (Beryllium) impurity and n-type

(Si) impurity simultaneously with the supply of Group III atoms (col 12, ln 35-50). Kobayashi et al also teaches the impurities are efficiently introduced at the lattice positions of the atoms of Group III and the doping was accomplished with a high degree of activation rate as compared with conventional MBE method (col 12, ln 35-50), this reads on supplying p-type and n-type impurity before the step of supplying the second raw material, thereby doping an impurity pair of the p-type and n-type into only the first layer.

As to the limitation "wherein a kind of impurity pairs composed of the p-type impurity raw material and the n-type impurity raw material are formed in the first layer" limitation, Kobayashi et al teaches supplying p-type (Beryllium) impurity and n-type (Si) impurity simultaneously with the supply of Group III atoms (col 12, ln 35-50); therefore this limitation is inherent. The limitation is inherent because Kobayashi et al teaches a similar method of supplying n-type and p-type raw materials, as applicant; therefore a similar method is expected to produce a material with similar properties. Also, it is noted that Applicant admits that if a lot of donor materials and acceptor materials are introduced at the same time, donor-acceptor complexes are formed in some small measure (See page 9, lines 8-9 of the remarks filed 6/22/2009); therefore since Kobayashi et al teaches p-type and n-type materials are supplied simultaneously, impurities pairs are inherently formed, as evidenced by applicant's admission.

Referring to claims 39, 41, Kobayashi et al teaches simultaneously supplying the p-type and n-type dopants (col 12, ln 35-50).

Referring to claims 40, 43 Kobayashi et al teaches simultaneously supplying p-type dopant, n-type dopant with the supply of Group III atoms (col 12, ln 35-50), this reads on supplying n-type and p-type dopant after starting the supply of the first crystal raw material.

Referring to claim 42, Kobayashi et al teaches Ga as the first crystal material and As as the second crystal material (col 10, ln 20-35).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 37-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishizawa et al (US 5,693,139) in view of Kobayashi et al (US 4,829,022).

Nishizawa et al discloses a method of growing doped semiconductor monolayers, note entire reference, comprising raw material gases of Gallium (Ga) and Arsenic (As), where Ga is supplied for 0.5 to 10 seconds, the chamber is evacuated, this clearly suggests applicant's purged for a predetermined time, and As is supplied for 2 to 200 seconds and the cycle is repeated (col

7, ln 1-67; col 8, ln 1-30 and Fig 7B and Fig 11). Nishizawa et al also discloses a p-type layer is formed by introducing an impurity gases and Ga simultaneously but alternately with an As source, where the impurity gas is an Mg, Zn or Cd containing gas or Silane. Nishizawa et al also discloses a n-type layer doped with Se or S and the impurity gas is introduced cyclically with the Ga gas and As gas or the impurity gas and Ga gas are introduced simultaneously but alternately with the As gas (col 8, In 31-60). Nishizawa et al also discloses forming pnp bipolar transistors (col 8, ln 61-67). Nishizawa et al also discloses nozzles 44, 45 and 46 for introducing gaseous compounds used for impurity doping for introducing group II, IV and VI gases (col 10, ln 50-67). Nishizawa et al also discloses different modes of doping, where the dopant is added at the exhaustion of an As gas, the introduction of a Ga gas, the exhaustion of a Ga gas or at the introduction of As gas (col 11-13 and Fig 11). Nishizawa et al also discloses other III-V semiconductors are applicable to the invention (col 14, ln 5-55). Nishizawa et al also discloses introduction of a Ga source gas and a group II dopant simultaneously to form a p-type layer (col 8, ln 30-45) and the introduction of a group IV dopant after the introduction of a Ga source gas (col 15, ln 5-50). Nishizawa et al also discloses selection of the timing of doping with respect of the source gas introduction is based on the desired dopant type for the monolayer being grown (col 15, ln 45-55). Nishizawa et al teaches supplying reactants for a short period of time (col 11, ln 50-60), this clearly suggests applicants pulsed manner. Nishizawa et al also teaches impurity sites in the crystal lattice can be controlled by selecting the introduction timing of the dopant gas. (col 13, ln 45-60).

Nishizawa et al does not disclose the given time for supplying each of the impurity raw materials are close to each other.

Kobayashi et al teaches Group III (Ga) atoms are supplied to the substrate so that one atomic layer is formed by one irradiation of the Ga beam (first crystal raw material) and then atoms of Group V (As) (second raw material) are supplied after the supply of Group III atoms has been completed, whereby the III-V molecules are formed (col 9, ln 25 to col 10, ln 51). Kobayashi et al also teaches the step of doping impurities which is required for the fabrication of various PN junction devices is carried out by supplying p-type (Beryllium) impurity and n-type (Si) impurity simultaneously with the supply of Group III atoms (col 12, ln 35-50). Kobayashi et al also teaches the impurities are efficiently introduced at the lattice positions of the atoms of Group III and the doping was accomplished with a high degree of activation rate as compared with conventional MBE method (col 12, ln 35-50), this reads on supplying p-type and n-type impurity before the step of supplying the second raw material, thereby doping an impurity pair of the p-type and n-type into only the first layer.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Nishizawa et al with Kobayashi et al's doping p-type and n-type impurities into the lattice positions of the atoms of the Group III atoms to achieve a high degree of activation.

Referring to claim 38, the combination of Nishizawa et al and Kobayashi et al does not teach supplying one of the n-type or p-type dopant after supplying the one of the n-type or p-type dopant. However, Nishizawa et al teaches doping a Ga layer by supplying a dopant while supplying Ga or after supplying Ga but before supplying As (Fig 11 and col 11, ln 25-60) and Nishizawa et al also teaches impurity sites in the crystal lattice can be controlled by selecting the introduction timing of the dopant gas. (col 13, ln 45-60). Therefore, It would have been obvious

to a person of ordinary skill in the art at the time of the invention to modify the combination of Nishizawa et al and Kobayashi et al to supplying one dopant during Ga deposition and the other dopant after the Ga deposition but before As is supplied, as suggest by Nishizawa, to control the impurity sites in the crystal lattice.

Referring to claims 39-43, see the remarks above in regards to the Kobayashi reference.

6. Claim 44 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nishizawa et al (US 5,693,139) in view of Kobayashi et al (US 4,829,022) as applied to claims 37-43 above, and further in view of Edmond et al (US 5,739,554) and Manabe et al (US 6,472,690).

The combination of Nishizawa et al and Kobayashi et al teaches all of the limitations of claim 44, as discussed previously, including using silane as a Si dopant and III-V compound semiconductors can be doped ('139 col 14, ln 1-25 nd col 13, ln 30-60). The combination of Nishizawa et al and Edmond et al does not teach the second raw material is NH_3.

Edmond et al teaches a III-V compound semiconductor gallium nitride (GaN) layer co-doped with both a Group II acceptor and Group IV donor (col 4, ln 50-67), where the group II acceptors include Zn or Mg and the Group IV donors include Si or Ge (col 6, ln 20-50), this clearly suggests applicant's time for supplying each of the impurity raw materials are close to each other. Edmond et al also discloses the GaN layer is formed by CVD, where Trimethylgallium (TMG), ammonia, silane and biscyclopentadienyl magnesium, $(Cp)_2Mg$ are used as reactant gases (col 7, ln 45-67 and col 8, ln 1-50). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Nishizawa et

al and Kobayashi et al with Edmond et al's co-doped GaN deposition with a second raw material NH_3 because the GaN layer is useful as an active layer (Abstract).

The combination of Nishizawa et al, Kobayashi et al and Edmond does not teach supplying TESi.

In a method of forming a gallium nitride compound semiconductor, note entire reference, Manabe et al teaches forming an n+ type Gallium nitride layer, using silane or tetraethylsilane (TESi) (Example 4). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Nishizawa et al, Kobayashi et al and Edmond with Manabe et al because substituting known equivalents for the same purpose is obvious (MPEP 2144.06).

Referring to claim 44, the combination of Nishizawa et al, Kobayashi et al, Edmond and Manabe et al teaches supplying the group III metal with a dopant or supplying a dopant after the Group III is supplied but before the group V element is supplied ('139 Fig 11); supplying n-type and p-type dopant into a Ga metal layer ('022 col 12, ln 35-50); using TESi as a dopant ('690 Example 4); and NH_3 as the group V material and $(Cp)_2Mg$ ('554 col 7, ln 45-67 and col 8, ln 1-50). The combination of Nishizawa et al, Kobayashi et al, Edmond and Manabe et al teaches forming III-V compound semiconductor by alternating cycles of Group III (TMG) and Group IV raw materials (NH_3) alternately to form monolayers (See '139 col 7, ln 1-65; '554 col 8, ln 10-20), which clearly suggests forming Ga as the first layer and N as the second layer

Response to Arguments

7. Applicant's arguments with respect to claims 37-44 have been considered but are moot in view of the new ground(s) of rejection.

8. Applicant's arguments filed 6/22/2009 have been fully considered but they are not persuasive.

Applicant's argument that Kobayashi et al does not disclose that a p-type and n-type impurity are supplied simultaneously is noted but not found persuasive. It is noted that applicant cites and underlines col 12, lines 38-47 of Kobayashi which teaches p-type impurity and Si as an n-type impurity were supplied simultaneously with the supply of atoms of Group III. Therefore, Kobayashi et al does teach p-type and n-type impurities supplied simultaneously. Kobayashi et al plainly states p-type and n-type impurities are supplied simultaneously with the Group III atoms to form PN junctions (col 12, ln 38-47). There is no basis for applicant's argument that this means supplying atoms of Group III which are the host with one of p-type impurity raw material and n-type impurity raw material. The Examiner's position that Kobayashi's teaching is form simultaneous introduction of n-type and p-type impurities is further evidenced by Edmond et al which teaches co-doping GaN with both acceptor and donor impurities to form pn junctions (col 4, ln 54-65).

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., doping techniques of the deep ultraviolet semiconductor device which can operate in the deep ultraviolet area) are not recited in the rejected claim(s). Although the claims are interpreted in light of the

specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant's argument against Edmond is noted but not found persuasive. Applicant alleges that the probability of forming the acceptor which is the state of the associating three atoms is low. However, applicant admits that Edmond et al teaches co-doping and if a lot of donor and acceptor materials are introduced at the same time, donor-acceptor complexes are formed in some small measure (pg 9, second full paragraph of the remarks filed 6/22/2009). Thus Edmond et al inherently teaches forming impurity pairs by codoping, as admitted by applicant.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MATTHEW J. SONG whose telephone number is (571)272-1468. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Kornakov can be reached on 571-272-1303. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Matthew J Song
Examiner
Art Unit 1792

MJS
10/25/09

/Matthew J Song/
Examiner, Art Unit 1792